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Final Technical Report
August 1999

REAL-TIME MULTICHANNEL AIRBORNE RADAR MEASUREMENT INTERFACE

ITT Systems

Dan Snell

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13. ABSTRACT *(Maximum 200 words)*
A real-time data interface was developed for the MCARM (Multi-Channel Airborne Radar Measurement) program. This report documents the interface hardware which was successfully developed, installed, and operated during flight tests to demonstrate onboard STAP (Space-Time Adaptive Processing). After installation on the BAC-111 flight test aircraft, the interface unit worked as designed without modifications.

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Executive Summary

ITT Systems is submitting this Final Report for Real-Time Multichannel Airborne Radar Measurement Interface. The results of this work allow processing of Multichannel Airborne Radar Measurement (MCARM) data through the use of specially designed hardware and software interfacing to UNIX hosts as well as other high performance computers.

ITT Systems assisted AFRL/Rome in developing the Real-Time MCARM interface board. This board provides a path from the VME-based host processor to a HIPPI interface. The HIPPI interface provides a generic connection to other boards and/or high performance computers. The HPC enables advanced algorithms to execute in real-time or near real-time on actual measurement data. This effort included the following tasks:

- Development of hardware for a VME to HIPPI interface
- Development of software for the VME based UNIX host
- Development of High Performance Computer (HPC) application software
- Development of network maintenance procedures and software

1. TECHNICAL APPROACH

1.1. Technical Discussion

The Multichannel Airborne Radar Measurement (MCARM) program allows AFRL/Rome to collect quality multichannel radar data from an airborne platform, for the study of clutter and adaptive processing algorithms. Real-time MCARM is AFRL/Rome in-house program for developing hardware and software to collect and process data in real-time or near real-time.

ITT Systems assisted AFRL/Rome in developing the Real-Time MCARM interface board that provides a path from the VME-based host processor to a HIPPI interface. The HIPPI interface provides a generic connection to other boards or high performance computers. The HPC enables studies of advanced algorithms executing in real-time or near real-time on actual measurement data. The following tasks were performed:

- Development of a printed circuit board for the interface between the VME based host processor and the HIPPI interface
- Development of software for the UNIX host
- Development of application software for the HPC
- Development of network maintenance procedures and software to permit the location and correction of network errors and topology

1.1.1. Technical Summary

ITT Systems accomplished the effort as follows:

1.1.2. Task 1: Hardware Development

A 9U VME card hosted the new printed circuit board developed for this project. The circuit for this board consists of an external input circuit, two memory buffers, a VME interface circuit, a Xilinx control circuit, and an external output circuit per channel (Figure 1-1). The MCARM board contains circuitry for four channels.

The input circuit receives 32 bits of synchronous data at a rate of 20 MHz. For the MCARM application, the data from a FFT board are considered 16I and 16Q data bits. However, this circuit can receive any 32 bit data words up to a 20 MHz rate. The incoming data is stored in a memory buffer. This buffer can be as large as 4 MegaWords, each word being 32 bits wide. When the buffer is full, a second memory buffer is switched in to handle the incoming data. This ping pong effect allows input data to be input continuously without interruption.

After a memory buffer is filled and switched to the output mode the VME host computer is notified. The VME host computer can manipulate the data as necessary. When the data is ready to be output the VME host computer starts the HIPPI data output interface. The data is sent to the HIPPI circuitry from the output memory buffer. The HIPPI interface circuit adds all the handshaking needed to implement the HIPPI data transfer.

The Xilinx Control circuit is the traffic cop of the interface. This circuit provides the control logic to store all the incoming data, switches the memory buffers when needed, directs data to and from the VME host, and controls the data going to the HIPPI interface. This circuit is programmable and has the capability to change how the interface works, thus allowing adaptability for other appellations.

The VME interface is provided to allow data manipulation during normal operation. It is also available for diagnostic testing. The VME host can read from any memory buffer or write data to any buffer for testing purposes. The VME bus can also write data to the HIPPI interface.

The MCARM interface card has 2 main modes of operation. These modes are set by a control word from the VME interface. The first mode is the normal data transfer mode. The other mode of operation is the diagnostic testing mode. The normal data transfer mode takes data from the FFT

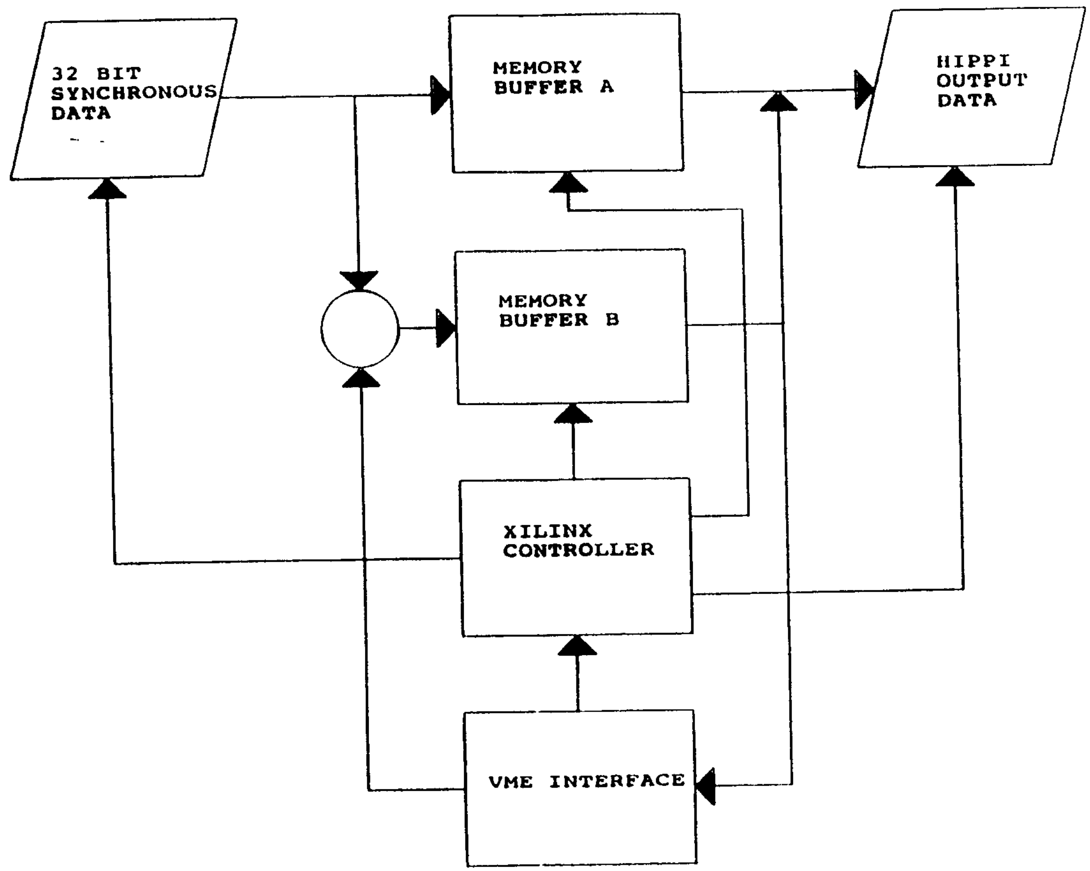


Figure 1-1: MCARM Printed Circuit Board Overview

board, buffers the data, adds control information to the data, and outputs the data to the HIPPI interface.

The diagnostic test mode actually consists of several modes. These diagnostic test modes are listed in the table below:

DIAGNOSTIC TEST MODES
▪ Read data from Memory Buffer A
▪ Read data from Memory Buffer B
▪ Write data to Memory Buffer A
▪ Write data to Memory Buffer B
▪ Reset circuit
▪ Write data to HIPPI Interface

The MCARM board detailed block diagram (Figure 1-2) is discussed in the following paragraphs. The 32 bit input data Catalina board is clocked into a data latch with the input clock. The inputs come into the board through an IDC connector – P50E-100P1-S1-TG at the end of the board. This connector is shared between 2 channels. The input data is sent to a data selector for data memory buffer A and B. The Zilinx Controller selects which Memory Buffer receives the data.

The Xilinx Controller also generates the address to the Memory Buffer for the incoming data. The Data in the other buffer is output to the HIPPI data buffer. The Xilinx Controller generates the Memory addressing and data selection for this output data. The XILINX controller initiates the data out to the HIPPI interface and monitors the status of the HIPPI interface. The XILINX controller monitors the control register generated by the VME interface and updates the VME status register as needed.

VME address and data can be selected for the Memory Buffers to allow reading and writing of data between the VME Bus and the Memory Buffers. Data is output through the HIPPI interface. The HIPPI data and controls signals are output on the same type 100 pin connector as the input data uses. The HIPPI interface does not share a connector between channels.

The Electrical Design and layout of this circuitry and assembly were performed by ITT Systems, State College, PA facility.

The PLD (22V10) and XILINX design was also performed by ITT Systems, State College.

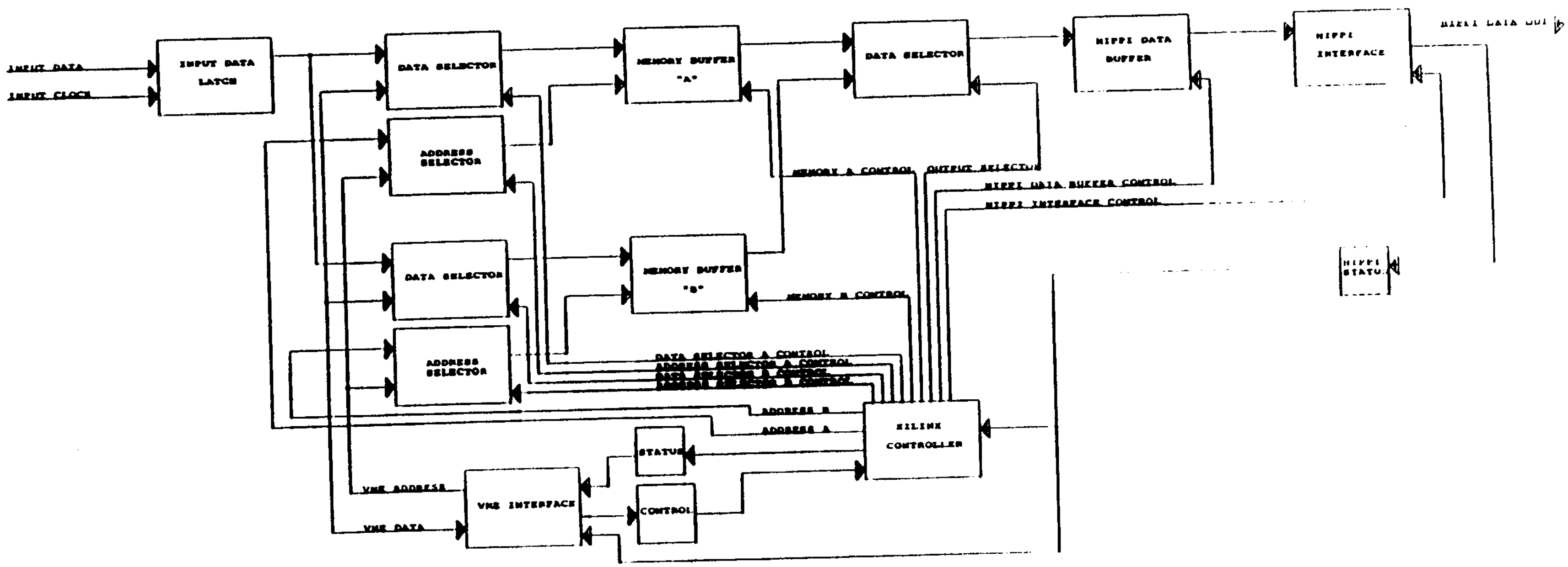


Figure 1-2: MCARM Printed Circuit Board Detailed Block Diagram

1.1.3. Task 2: Software Development

ITT Systems developed the software for the VME host computer to coordinate data transfer between the MCARM PCB data buffers and the HIPPI interface. The software was developed to take full advantage of the MCARM PCB's double memory buffers, thus allowing an uninterrupted 32 bit synchronous data flow.

The VME host software performs required data manipulation as well as monitoring status, mode selection and control of the MCARM PCB.

Diagnostic software was developed to test the operation of the MCARM PCB using the diagnostic mode feature of the board. Tests included read/write memory test of the A and B buffers, reset test, and HIPPI interface test.

Additional VME host computer software was also developed to interface with PCB's other than the MCARM PCB. An example of this is the FFT board that was used in conjunction with the MCARM PCB to provide the 32 bit synchronous data to be processed by the MCARM board.

1.1.4. Task 3: High Performance Computer Interface

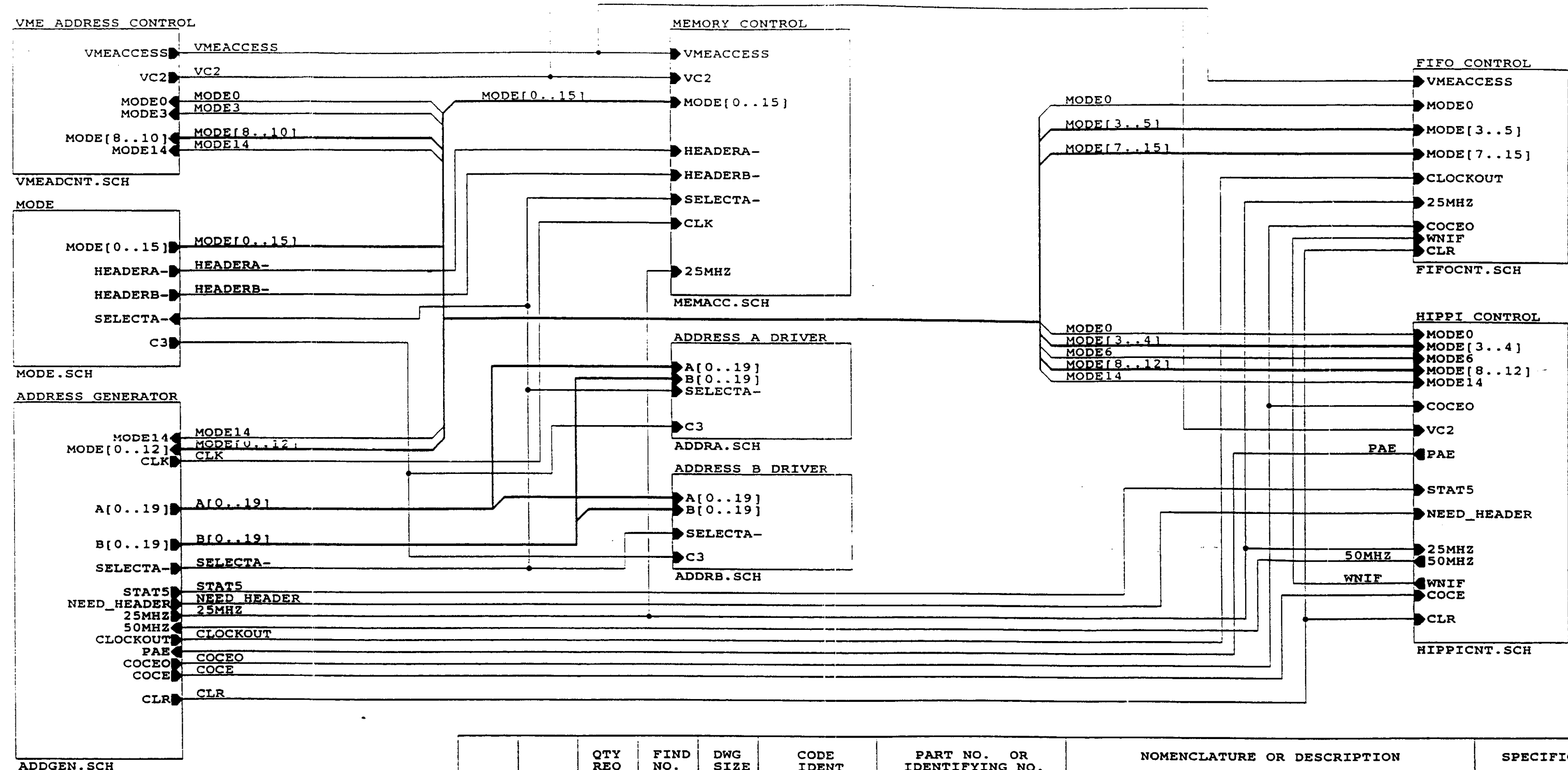
The MCARM PCB HIPPI was interfaced with the HPC. Required software was developed for the AFRL/Rome HPC to support the MCARM PCB to HPC interface.

1.1.5. Task 4: Network Maintenance

ITT Systems supported the integration of the HPC onto the AFRL/Rome network. This included the configuration of the network, and development of procedures and software to ensure proper network operation, and to isolate and fix network problems as they arise.

Appendix A

FPGA Schematics



QTY REQ	FIND NO.	DWG SIZE	CODE IDENT	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	NOTES

PARTS LIST

DIMENSION IN INCHES		DRAWN BY	DATE
TOLERANCES			
FRACTIONS	DECIMALS	CHKD	
	.XX	CHKD	
ANGLES	.XXX	APVD	
		APVD	

FILE

DISK

MATERIAL | FINISH

DWG SIZE | NEXT ASSY | USED ON

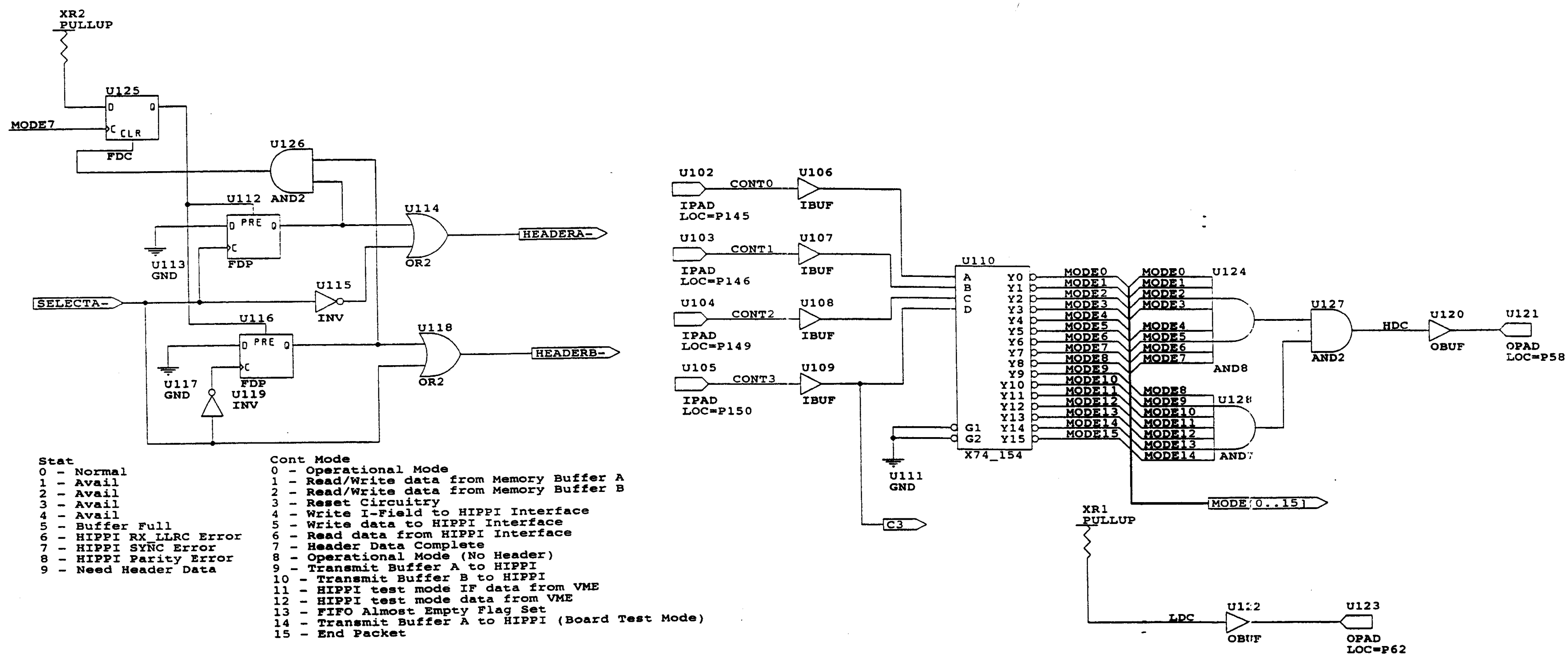
APPLICATION

LOCUS, INC. STATE COLLEGE, PA

MCARM FPGA

SIZE	CODE IDENT	DWG NO.
B	50311	

SCALE	CONTRACT NO.	SHEET
		1 of 9



Stat
0 - Normal
1 - Avail
2 - Avail
3 - Avail
4 - Avail
5 - Buffer Full
6 - HIPPI RX_LLRC Error
7 - HIPPI SYNC Error
8 - HIPPI Parity Error
9 - Need Header Data

Cont Mode
0 - Operational Mode
1 - Read/Write data from Memory Buffer A
2 - Read/Write data from Memory Buffer B
3 - Reset Circuitry
4 - Write I-Field to HIPPI Interface
5 - Write data to HIPPI Interface
6 - Read data from HIPPI Interface
7 - Header Data Complete
8 - Operational Mode (No Header)
9 - Transmit Buffer A to HIPPI
10 - Transmit Buffer B to HIPPI
11 - HIPPI test mode IF data from VME
12 - HIPPI test mode data from VME
13 - FIFO Almost Empty Flag Set
14 - Transmit Buffer A to HIPPI (Board Test Mode)
15 - End Packet

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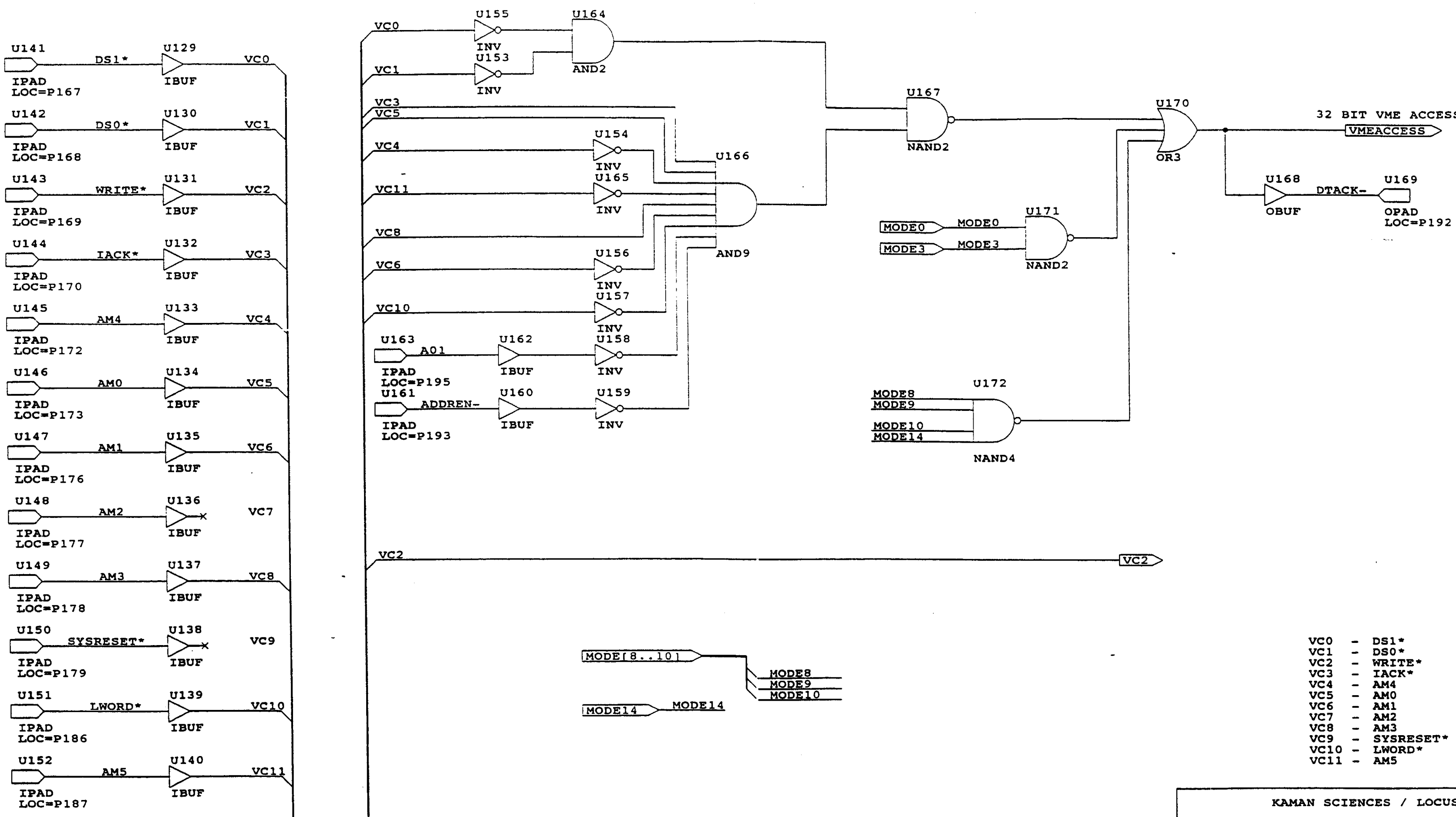
Title	MODE
Size B	Document Number	REV
Date: December 11, 1995	Sheet 2 of 9

VMEACCESS = !DS1* & !DS0* & IACK* & ((AM[5..0]==001001b) & (AM[5..0]==001101b)) & !LWORD* & !A01 & !ADDREN*



VC0 - DS1*
VC1 - DS0*
VC2 - WRITE*
VC3 - IACK*
VC4 - AM4
VC5 - AM0
VC6 - AM1
VC7 - AM2
VC8 - AM3
VC9 - SYSRESET*
VC10 - LWORD*
VC11 - AM5

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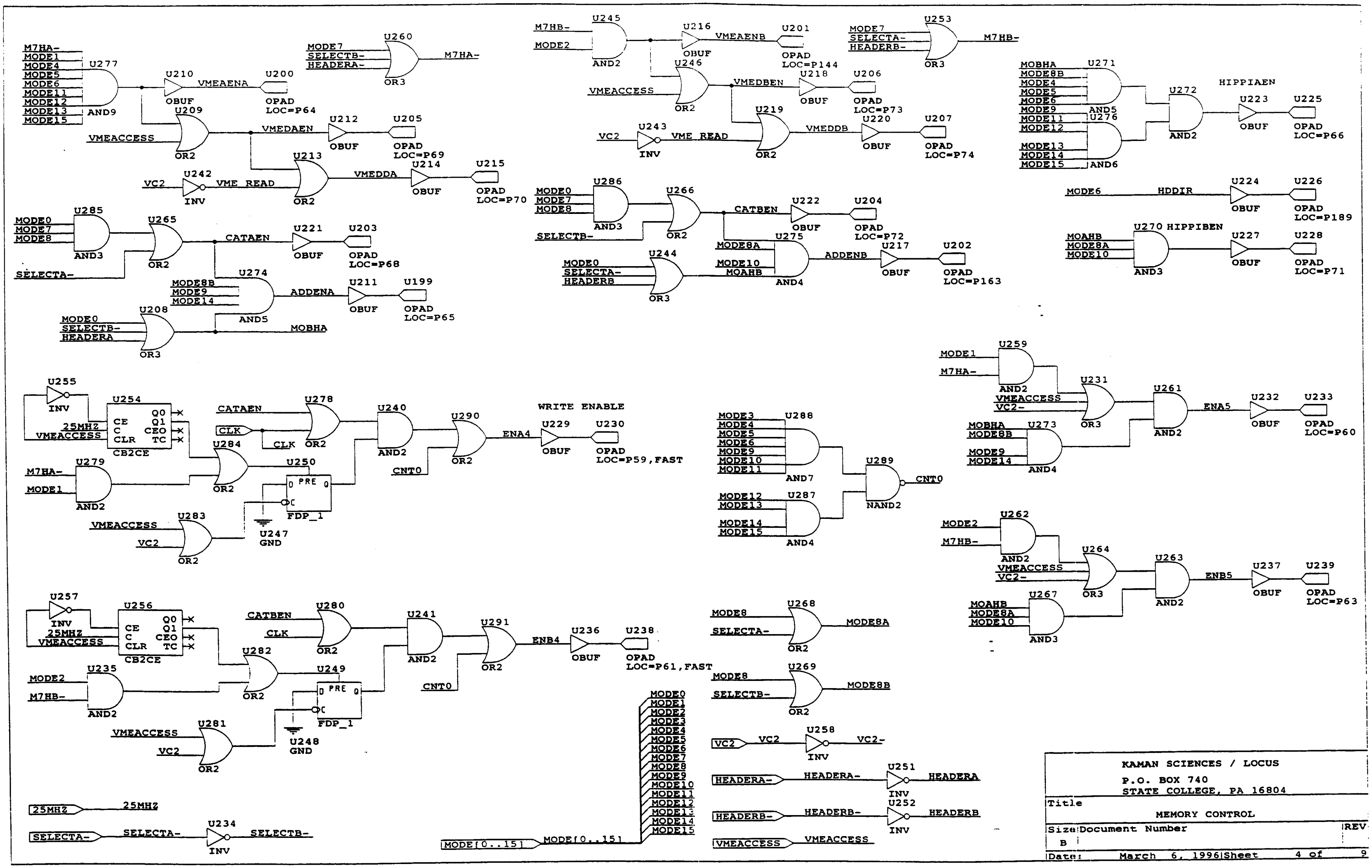
Title: VME ADDRESS CONTROL

Size: B | Document Number | REV

Date: December 11, 1995 Sheet 3 of 9



KAMAN SCIENCES / LOCUS P.O. BOX 740 STATE COLLEGE, PA 16804	
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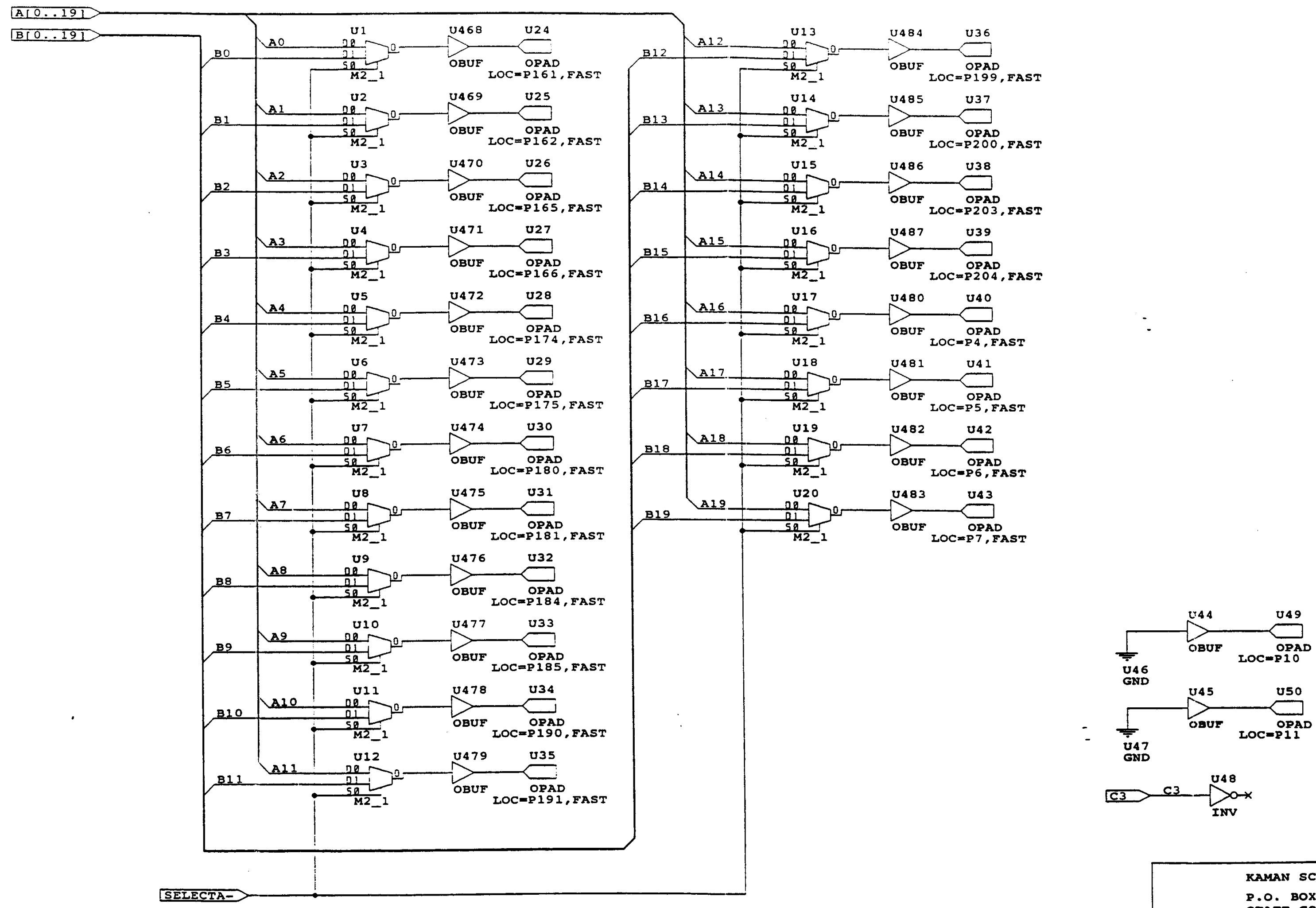
Size: B	Document Number	REV
Date: March 6, 1996	Sheet 4 of 9



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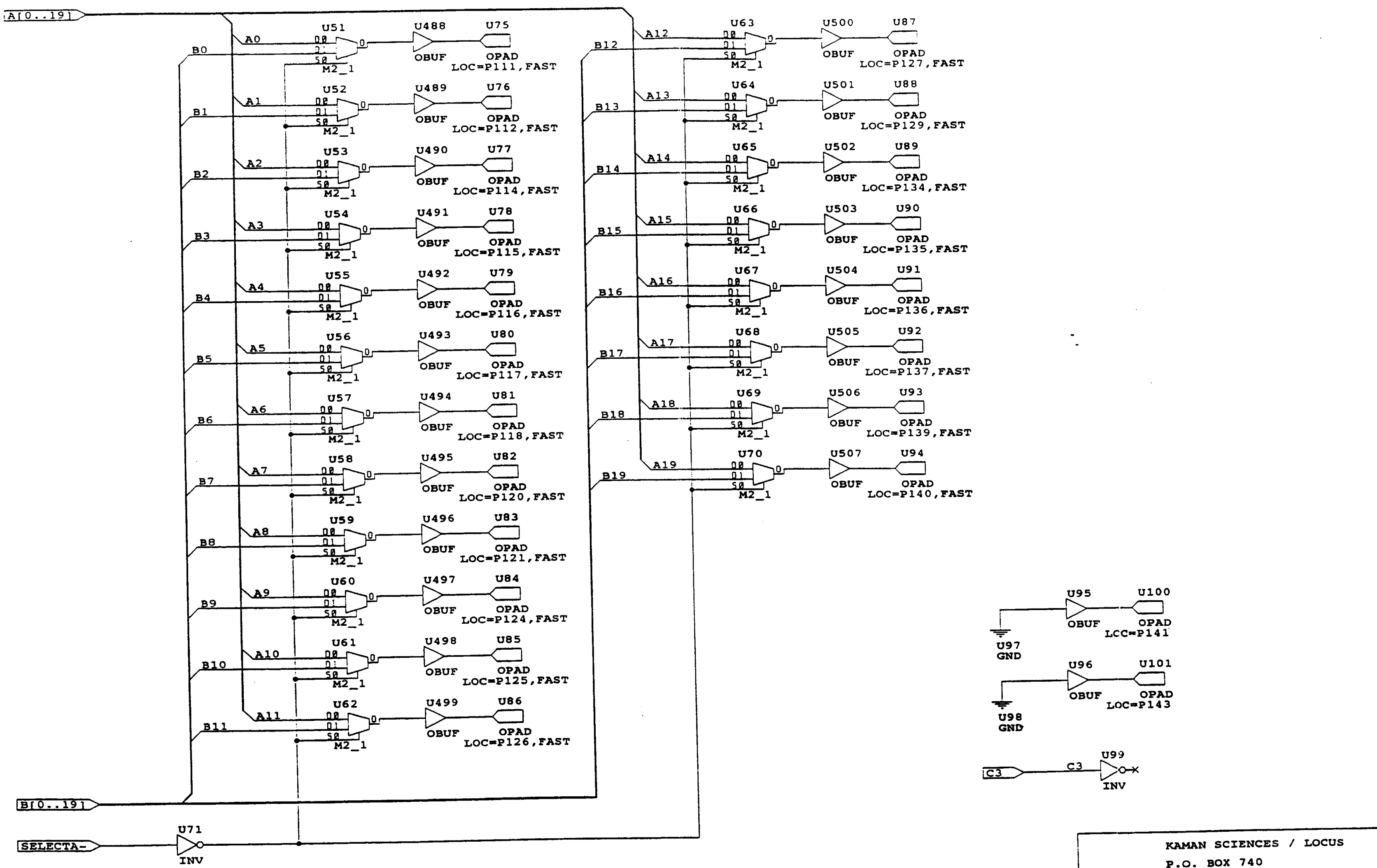
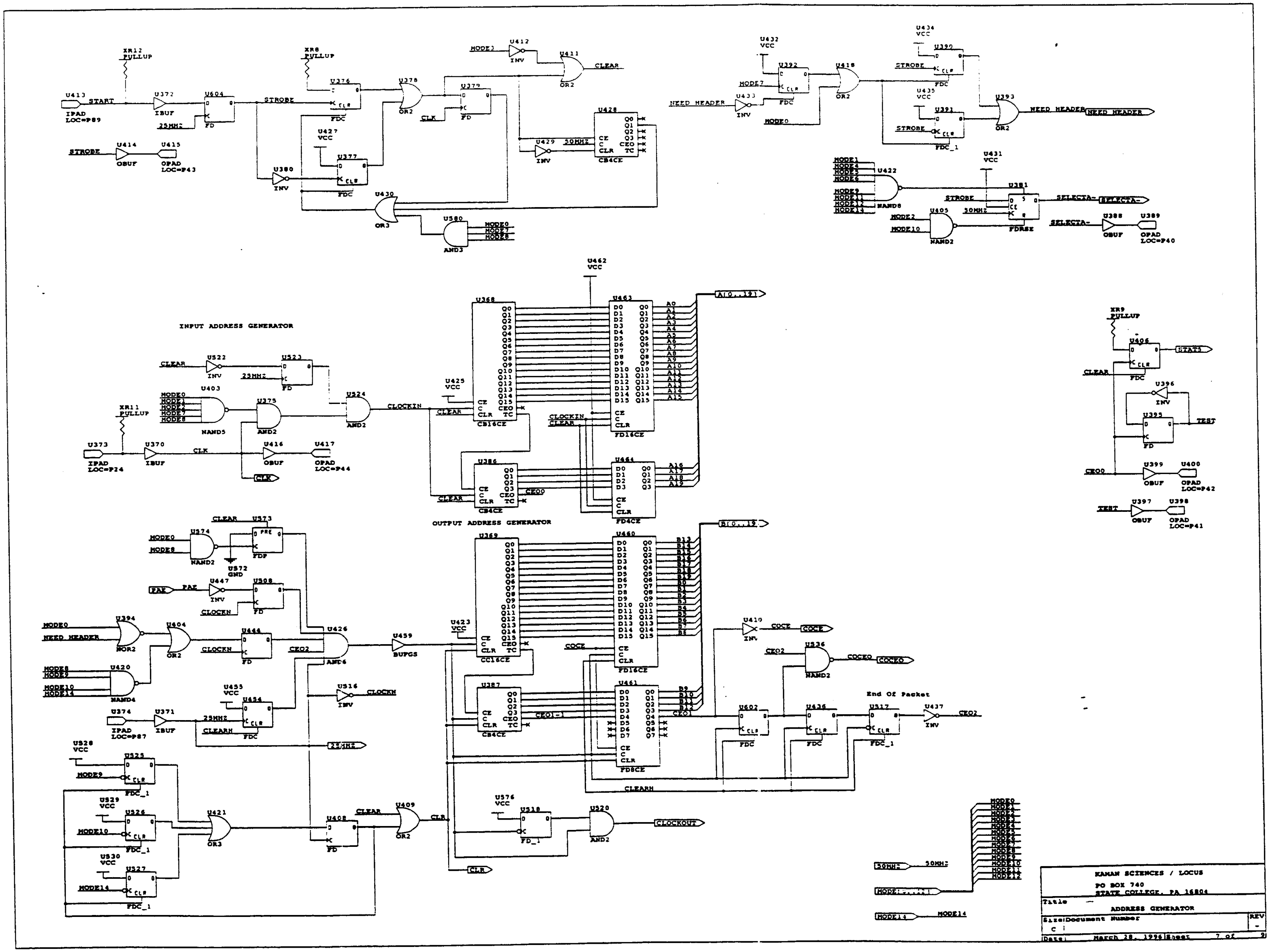
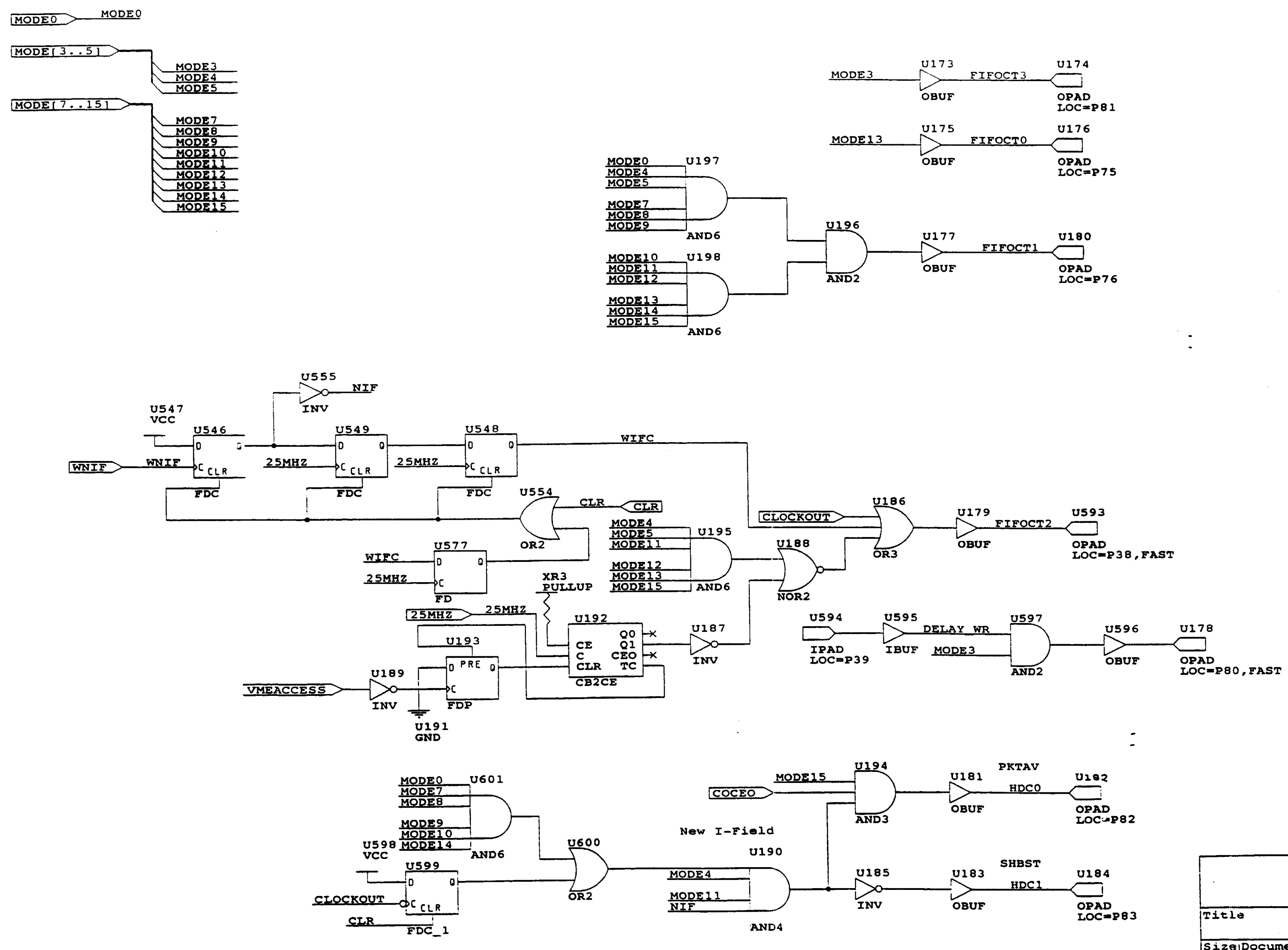
Title	BUFFER A ADDRESS DRIVER	
Size B	Document Number	REV
Date: December 21, 1995	Sheet 5 of 9	



KAMAN SCIENCES / LOCUS P.O. BOX 740 STATE COLLEGE, PA 16804	
Title BUFFER B ADDRESS DRIVER	
Size Document Number B	REV
Date: December 21, 1995 Sheet 6 of 9	


INPUT ADDRESS GENERATOR
OUTPUT ADDRESS GENERATOR
End Of Packet
KAMAN SCIENCES / LOCUS
PO BOX 740
STATE COLLEGE, PA 16804
Title
ADDRESS GENERATOR
Size Document Number
C
REV
Date: March 28, 1996 Sheet 7 of 9



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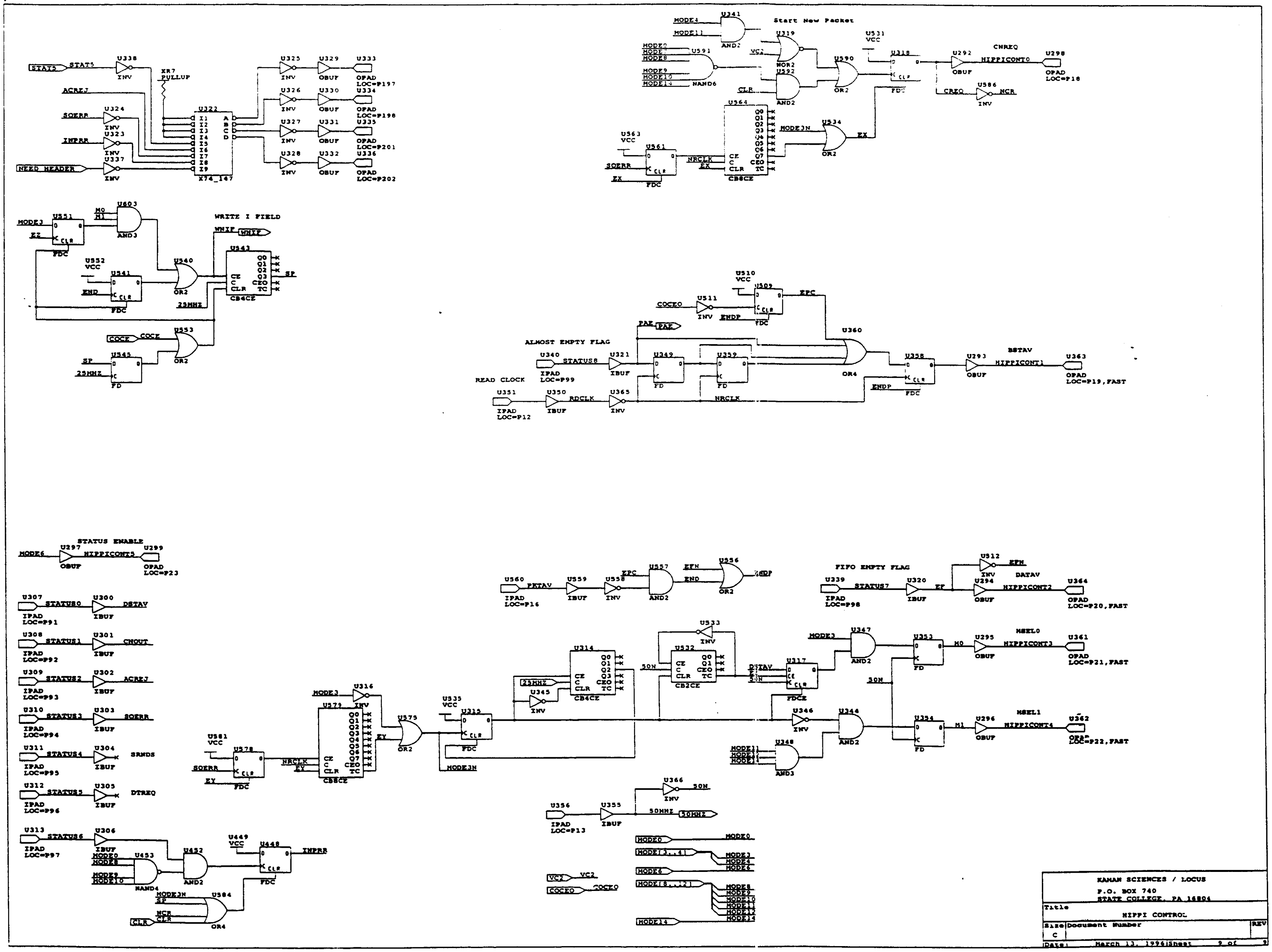
Title	FIFO CONTROL
Size B	Document Number	REV
Date: March 13, 1996	Sheet 8 of 9


Start New Packet
WRITE I FIELD
ALMOST EMPTY FLAG
READ CLOCK
STATUS ENABLE
FIFO EMPTY FLAG
KAMAN SCIENCES / LOCUS
P.O. BOX 740
STATE COLLEGE, PA 16804
Title
HIPPI CONTROL
Size
Document Number
REV
C
Date:
March 13, 1996
Sheet
9 of 9